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MULTI-PURPOSE LOW-NOISE CHARGE AMPLIFIER

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ABSTRACT

Semi-conductor detectors, photo-diodes, low-gain proportional gas counters need low-noise charge amplifiers under high input capacitance. The amplifier described here has a RMS noise level of 460 e^- at 20 pF input capacitance, 20 ns output rise time, and 100 ns gate width; 130 e^- RMS noise at 0 pF and 2 µs - 2 µs shaping time with a slope of 4 e^-/pF. In addition, a complete amplification stage with 2 MHz counting rate capability is described.

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1. CIRCUIT DESCRIPTION

For an amplifier coupled to a radiation detector, these characteristics are of importance: capacitance, charge collection time and the available output charge.

An amplifier with a rise time of about 10 ns and a time constant of several tenths of µs must be made of FET input transistors and cover a large variety of collection times, from the fastest silicon strip detector and wire chamber to the slowest scintillation detector. In addition the use of a large feedback resistor eliminates parallel noise.

In order to keep the best signal-to-noise ratio with high capacitance detectors, it is necessary to have the highest open loop gain. This can be done by increasing the number of transistors in the amplifier, but care must be taken in the choice of those transistors and in the layout of the printed circuit board; in both cases parasitic capacitance and self-inductance could introduce phase shift which generally means oscillation, particularly when there is no input capacitance. The choice of the input transistor can permit a good adaptation to the detector capacitance without increasing the power consumption. One can now find on the market FET's with a transconductance of 40 nS under a drain current less than 10 mA which makes it possible to increase the open-loop gain and minimize the capacitance dependence. The circuit diagram of Fig. 1 makes an attempt to put all these features together.

The choice of an input transistor from 10 mS (J309) to 40 mS (2SK147) transconductance, and with a constant current flow of 7 mA, makes it well matched to detectors from a few pF to a few nF. The output buffer of the amplifier gives ± 2 V linear on 50 Ω and ± 6 V on 1 kΩ. In order to keep the amount of components as low as possible, and because this type of amplifier always needs special shaping like delay-line shaping (cf 2) or pole-zero cancellation, the output temperature coefficient has not been considered. This should permit a lower hybridation price.

Actually, the printed-circuit board is available with a possibility to choose between two types of use. One has semi-conductor detectors or photo-diodes with a bias input accepting up to 200 V bias voltage and no spark protection; the other one has no bias voltage but a spark protection up to 3 kV (100 pF). All other kinds of input can be done. The price for an amplifier mounted on printed circuit is at present 15.– SF.

2. PEROFRMANCE CHARACTERISTICS

- Sensitivity : 450 mV/pC, 2.2 pF feedback (see Fig. 3)
- Output rise-time: 14 ns (see Fig. 7)
- Output decay-time: (10%-10%): 500 µs
- Noise related to the input: 460 e^- RMS with 20 ns rise-time, 20 pF input capacitance and 100 ns gate width (see Figs 4,5 and 6)
- 130 e^- at 0 pF and 2^- µs - 2 µs shaping time (extrapolated point, see Fig. 4).
- Output dynamic range: ± 10000 or 2.0 V/50 Ω load
  ± 30000 or 6 V/1K Ω load
  This can be extended to 50000 on 50 Ω by a special choice of internal bias and transistors.
- Output off-set : can be trimmed to 0,000 V, but the temperature coefficient being 1 mV/°C, this can be improved by adding active components.

3. COMPLETE 2 MHz AMPLIFIER STAGE

This stage (Fig. 2) is made of a pre-amplifier like the one described above, followed by an operational amplifier and a 50 Ω driver. The output of the pre-amplifier goes directly into the inverting input, the other one goes into the non-inverting input through a delay line. The operational amplifier takes the difference which is equivalent to the first part of the incoming signal with a width equal to the delay of the delay line. This gives a signal with a rectangular shape when the gain is the same on the two inputs of the operational amplifier; another advantage is a complete freedom from the output DC level of the pre-amplifier and its temperature coefficient.

With an operational amplifier such as the Harris Ha-5195, and an output shaping time of 200 ns (Fig. 8), the performance can be the following (both together):

- sensitivity up to 5 V/pC,
- noise RMS: 500 e^- (20 pF at the input, 100 ns gate),
- rise-time: 20 ns,
- linear output dynamic range up to 5 V/50 Ω,
- DC output level temperature coefficient 100 µV/°C,
- 2 MHz repetition rate.

FIGURE CAPTIONS

Fig. 1: Complete circuit diagram of the charge amplifier.

Fig. 2: Complete circuit diagram of the 2 MHz counting rate amplifier stage.

Fig. 3: Curves showing the dependence of the rise-time and the sensitivity to the input capacitance.

Fig. 4: Curves showing the dependence of the input noise with the input capacitance at different shaping time and gate width.

Fig. 5: Noise contribution with the following conditions:
- 20 pF input capacitance,
- 20 ns rise-time,
-200 ns rectangular shaping time (see Fig. 8),
-100 ns gate width centered on the output width.
1 Femto C between peaks - 460 e^- RMS.

Fig. 6: Noise contribution with the following conditions:
-20 pF input capacitance,
-200 ns - 200 ns shaping time,
-300 ns gate width.
1 Femto C between peaks - 350 e^- RMS.

Fig. 7 Output rise-time of the charge amplifier with 20 pF input capacitance.

Fig. 8: This photo shows the possibility to separate events with the amplifier of the Fig. 2.

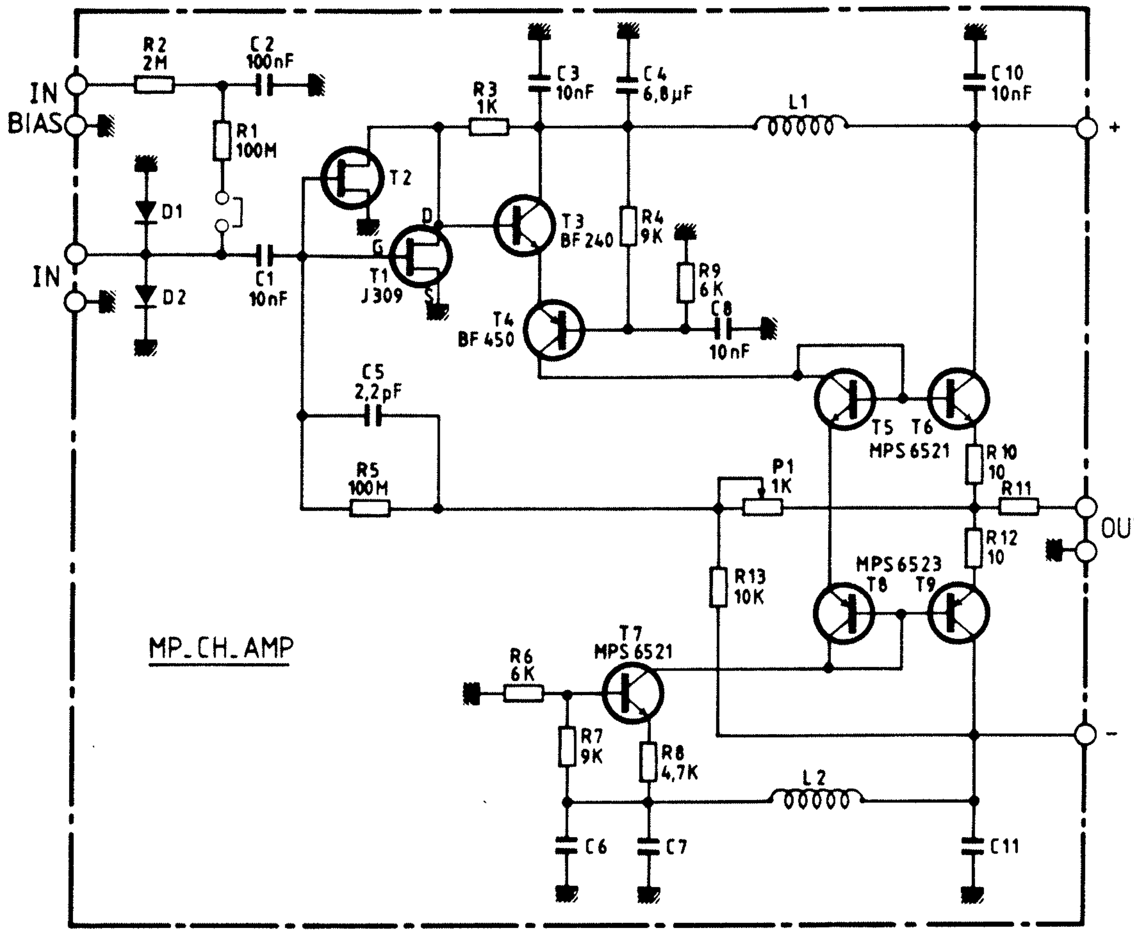
IN
BIAS
IN
R2
2M
C2
100nF
R1
100M
D1
D2
C1
10nF
T2
T1
J309
G
D
S
R3
1K
C3
10nF
C4
6,8μF
L1
C10
10nF
+
T3
BF240
R4
9K
R9
6K
C8
10nF
T4
BF450
C5
2,2pF
R5
100M
T5
T6
MPS6521
R10
10
P1
1K
R11
OUT
R12
10
MPS6523
T8
T9
R13
10K
MP_CH_AMP
T7
MPS6521
R6
6K
R7
9K
R8
4,7K
L2
C6
C7
C11
-

Fig. 1

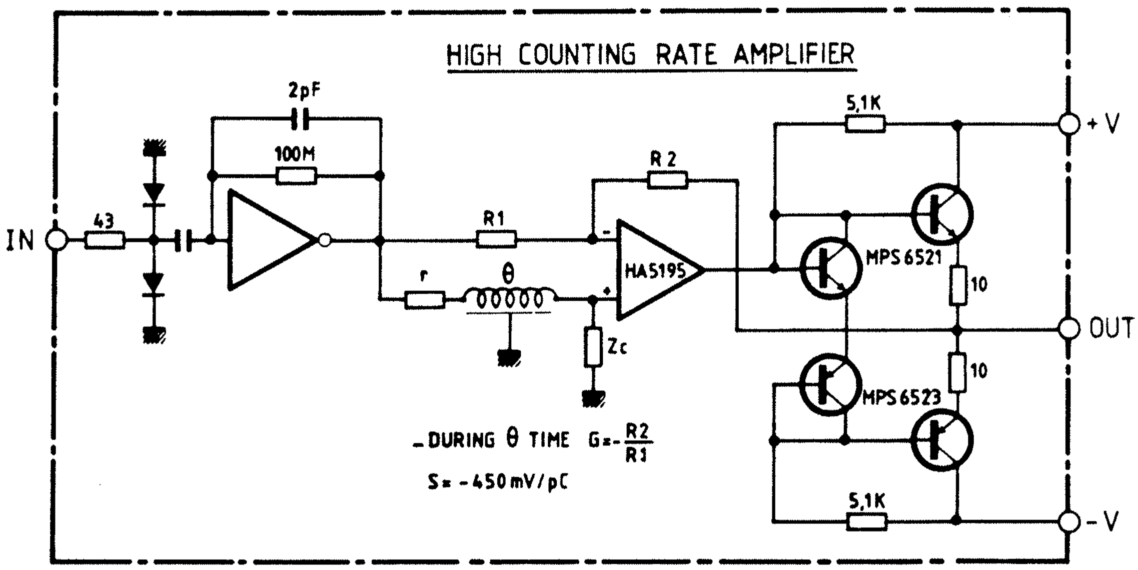
HIGH COUNTING RATE AMPLIFIER
2pF
100M
IN
43
R1
R2
r
θ
HA5195
Zc
5,1K
+V
MPS6521
10
OUT
10
MPS6523
5,1K
-V
_DURING θ TIME G=-R2/R1
S= -450mV/pC

Fig. 2

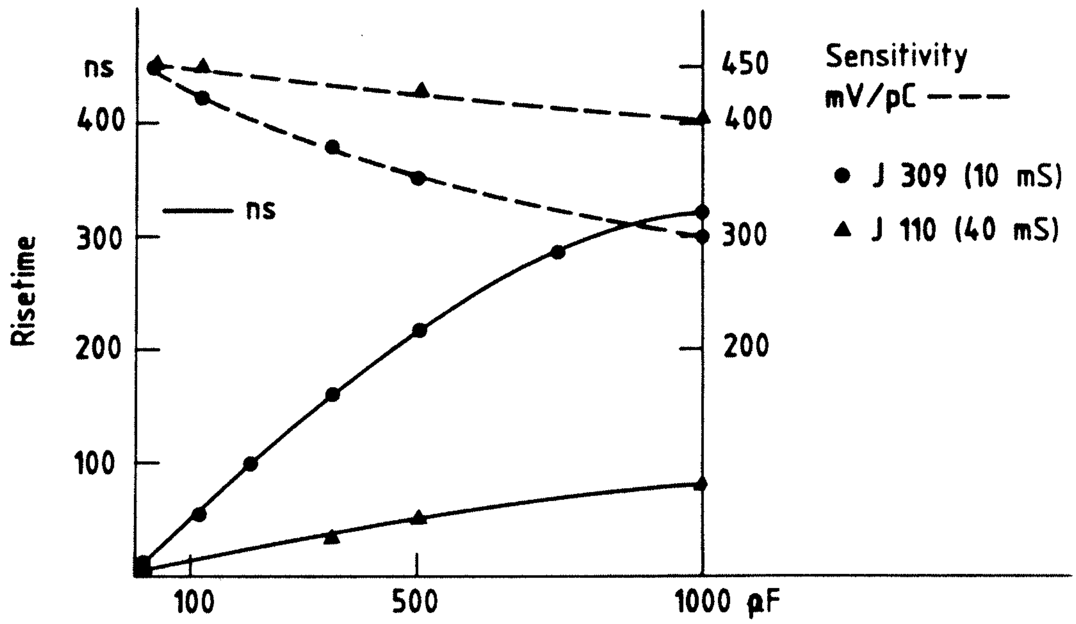
ns
400
300
200
100
Risetime
— ns
450
400
300
200
Sensitivity
mV/pC ---
● J 309 (10 mS)
▲ J 110 (40 mS)
100
500
1000 pF

FIG. 3

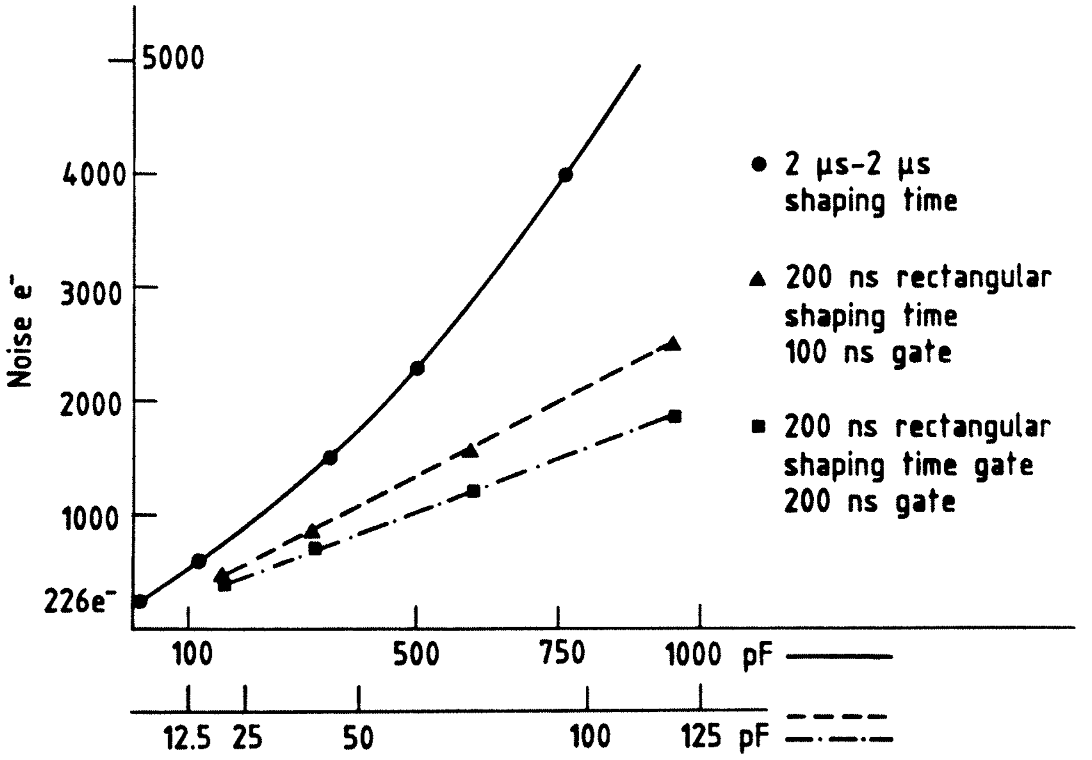
5000
4000
3000
2000
1000
226e⁻
Noise e⁻
● 2 µs-2 µs
shaping time
▲ 200 ns rectangular
shaping time
100 ns gate
■ 200 ns rectangular
shaping time gate
200 ns gate
100
500
750
1000 pF
12.5
25
50
100
125 pF

FIG. 4

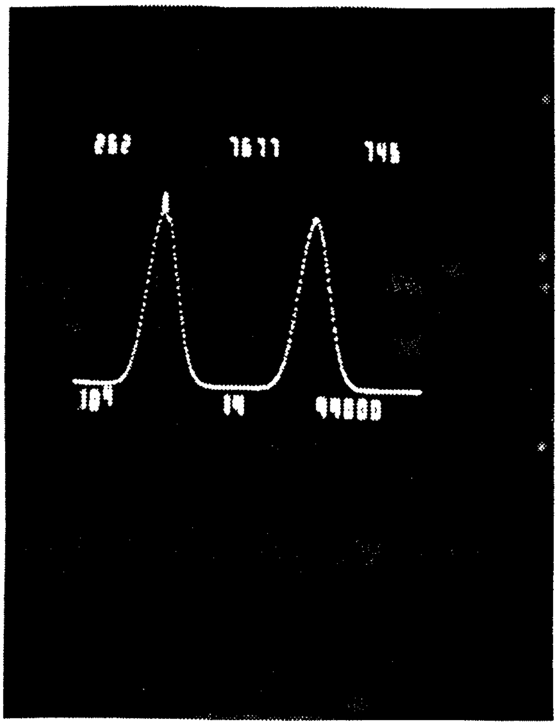

Fig. 5

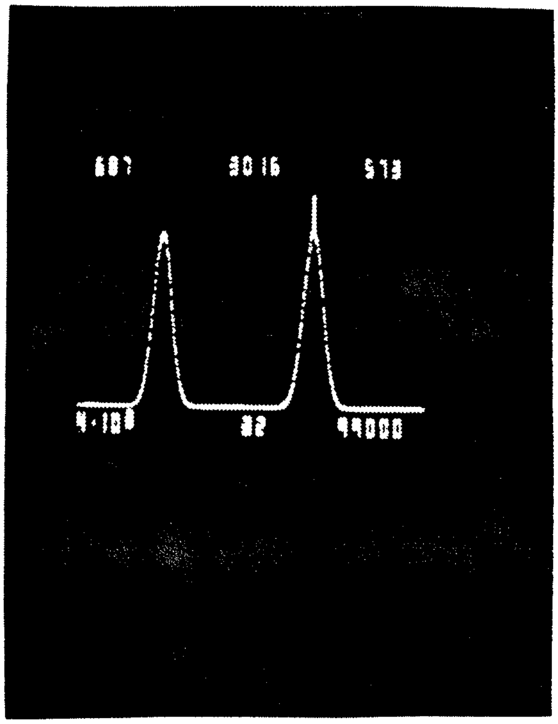

Fig. 6

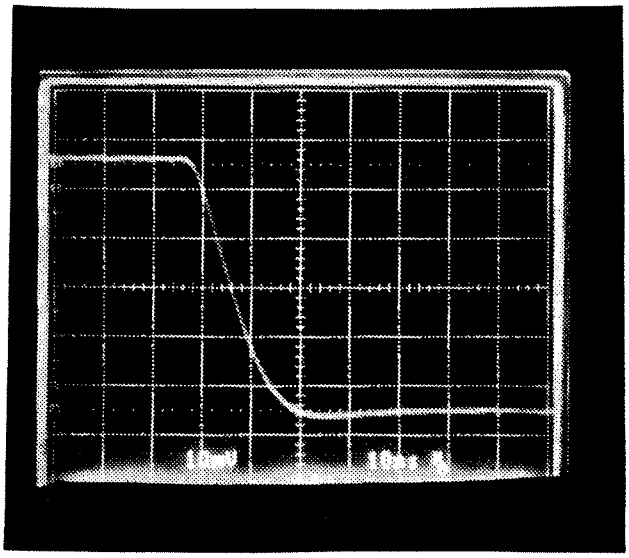

Fig. 7

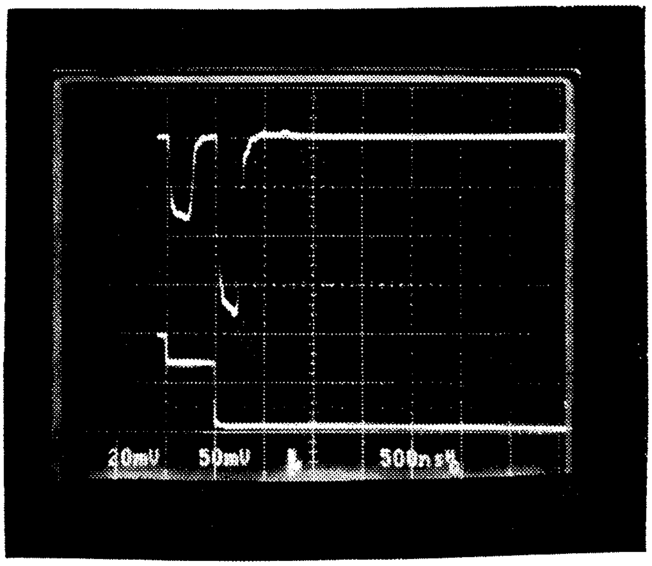

Fig. 8